CLAIMS

What is claimed is:

1. A memory system having a plurality of memories each having a command decoder front end receiving incoming command packets, and a set of at least one command sequencer,

wherein said command decoder front end has facilities for (1) at least partially decoding incoming command packets, (2) issuing commands to at least one sequencer in said set of command sequencers in response to said incoming command packets, and (3) performing a first group of at least one memory control step of a decoded command in response to said incoming command packets,

and wherein each of said command sequencers has facilities for performing a second group of memory control steps of decoded commands issued to the command sequencer from the command decoder front end.

2. A system according to claim 1, wherein said command decoder front end further has facilities for assembling each of said incoming command packets from a respective plurality of consecutive incoming command words.

3. A system according to claim 1, wherein said command decoder front end further has facilities for

determining whether or not to perform said first group of memory control steps for a given incoming command packet.

4. A system according to claim 1, wherein each of said incoming command packets has associated therewith a respective desired latency value, and wherein said command decoder front end further has facilities for performing said first group of memory control steps for a given incoming command packet only if the desired latency value associated with said given command packet is below a predetermined threshold latency value.

5. A system according to claim 4, wherein each of said command sequencers further has facilities for performing said first group of memory control steps for said given incoming command packet, if said command decoder front end does not perform said first group of memory control steps for said given incoming command.

6. A system according to claim 4, wherein said incoming command packets include a command type indicator, and wherein said command decoder front end includes facilities to determine the desired latency value for the given command packet in dependence upon the command type indicator in the given command packet.

7. A system according to claim 1, wherein the facilities of said command decoder front end for issuing commands to at least one sequencer in response to said incoming command packets, issues such commands for a given incoming command packet substantially simultaneously with the performance by said command decoder front end of a memory control step for said given incoming command packet.

8. A method for managing a memory system, for use with an incoming command packet, comprising the steps of:

receiving said incoming command packet in a command decoder front end;

said command decoder front end decoding said command packet, issuing a command to a first command sequencer in response to said command packet, and further performing a first group of at least one memory control step in response to said incoming command packet; and

said first command sequencer performing a second group of at least one memory control step in response to receipt of said command from said command decoder front end.

9. A method according to claim 8, further comprising the step of assembling said command packet from a plurality of consecutive incoming command words.

10. A method according to claim 8, further comprising the step of said first command sequencer determining that said first group of memory control steps, are performed by said command decoder front end,

further comprising the step of said first command sequencer abstaining from performing said first group of memory control steps in response to said step of determining.

11. A method according to claim 8, wherein said step of said command decoder front end issuing a command to a first command sequencer in response to said incoming command packet occurs substantially simultaneously with the step of said command decoder front end performing a first group of at least one memory control step in response to said incoming command packet.

12. A method according to claim 8, further comprising the steps of:

said command decoder front end further indicating a latency value to said first command sequencer in

conjunction with said step of said command decoder issuing a command to a first command sequencer; and

said first command sequencer inserting at least one latency wait state in dependence upon said latency value indicated by said command decoder front end, after receipt of said command from said command decoder front end and prior to said step of performing a second group of at least one memory control step.

13. A method according to claim 8, further comprising the step of said command decoder front end selecting said first command sequencer from among a plurality of parallel command sequencers in response to receipt of said command packet.

14. A method for managing a memory system, for use with a first incoming command packet, comprising the steps of:

receiving said first incoming command packet in a command decoder front end;

said command decoder front end decoding said first command packet, issuing a command to a first command sequencer in response to said first command packet, and determining whether to perform a first group of at least

one memory control step in response to said first command packet; and

said first command sequencer performing a second group of at least one memory control step in response to receipt of said command from said command decoder front end.

15. A method according to claim 14, further comprising the step of assembling said command packet from a plurality of consecutive incoming command words.

16. A method according to claim 14, wherein said command decoder front end determines to perform said first group of memory control steps, further comprising the step of said command decoder front end performing said first group of memory control steps in response to said first command packet,

wherein said second group of memory control steps excludes said first group of memory control steps.

17. A method according to claim 16, wherein said step of said command decoder front end issuing a command to a first command sequencer in response to said first command packet occurs substantially simultaneously with said step of said command decoder front end performing said first

group of memory control steps in response to said first command packet.

18. A method according to claim 14, wherein each of said incoming command packets has associated therewith a respective desired latency value, and wherein said command decoder front end performs said step of determining whether to perform said first group of memory control steps in response to a determination of whether the desired latency value associated with said first command packet is below a predetermined threshold latency value.

19. A method according to claim 18, wherein said command decoder front end determines that the desired latency value associated with said first command packet is below said predetermined threshold latency value, further comprising the step of said command decoder front end performing said first group of memory control steps in response to said first command packet,

wherein said second group of memory control steps excludes said first group of memory control steps.

20. A method according to claim 18, wherein said command decoder front end determines that the desired latency value associated with said first command packet is

not below said predetermined threshold latency value, further comprising the step of said first command sequencer performing said first group of memory control steps in response to receipt of said command from said command decoder front end.

21. A method according to claim 18, wherein said incoming command packets include a command type indicator, further comprising the step of wherein said command decoder front end determining the desired latency value for said first command packet in dependence upon the command type indicator in the first command packet.

22. A method according to claim 14, further comprising the steps of:

said command decoder front end further indicating a latency value to said first command sequencer in conjunction with said step of said command decoder issuing a command to a first command sequencer; and

said first command sequencer inserting at least one latency wait state in dependence upon said latency value indicated by said command decoder front end, after receipt of said command from said command decoder front end and prior to said step of performing a second group of at least one memory control step.

23. A method according to claim 14, further comprising the step of said command decoder front end selecting said first command sequencer from among a plurality of parallel command sequencers in response to receipt of said command packet.

24. A method of operating a memory device for use in a packet-driven memory system comprising the steps of:

receiving external command packets in a command front end circuit;

decoding said external command packets into internal commands in said command front end circuit;

issuing said internal commands to respective selected ones of a plurality of command sequencers;

receiving each of said internal commands from the command front end circuit into the respective selected sequencer;

performing a first group of control steps for a respective given internal command decoded from each given one of said external command packets, either in the command front end circuit or in the sequencer selected for the given internal command, selectably in dependence upon a comparison of a latency value associated with the given external command packet with a threshold latency value; and

performing a second group of control steps for the given internal command in the sequencer selected for the given internal command.

25. A method according to claim 24, further comprising the steps of:

receiving in the command sequencer selected for each given internal command a latency indication from the command front end circuit; and

entering a wait state for a selected number of clock cycles in dependence upon the command delay indication for each given internal command, after receipt of the given internal command in said step of receiving internal commands, and prior to said step of performing a second group of at least one memory control step.

26. A method for processing commands in a memory system having a command module and multiple memory modules coupled together via command and data links, the method comprising the steps of:

issuing a command packet from the command module to a selected memory module, the command packet having a latency value associated therewith;

receiving the command packet in the selected memory module via a command decoder front end;

decoding the issued command packet into an internal command;

internally issuing the decoded command to a selected one of a plurality of parallel functional units;

performing a first group of control actions in the command decoder front end if the latency value is less than a predetermined latency threshold; and

performing a remaining group of control actions in the selected parallel functional unit.

27. A method of operating a memory device for use in a packet-driven memory system comprising the steps of:

receiving external command packets in a command front end circuit;

decoding one of the external command packets to produce an internal command in the command front end circuit;

issuing the internal command to a selected one of a plurality of command sequencers;

performing a first group of control steps in the command front end circuit;

receiving the internal command from the command front end circuit into the selected sequencer;

receiving a command delay output from the command front end circuit into the selected sequencer;

entering a wait state for a selected number of clock cycles if a latency value associated with the internal command is greater than a predetermined latency threshold, and

executing remaining control steps in the selected command sequencer.

28. A method for generating a control signal delayed by a delay time specified with a resolution smaller than one period of a clock signal, comprising the steps of:

receiving a desired delay time specified as a digital delay value which includes an m-bit integral multiple and an n-bit fractional multiple of the period of said clock signal, m>0 and n>0;

loading said m-bit integral multiple into a counter clocked synchronously with said clock signal;

generating said control signal in response to count completion of said counter; and

further delaying said control signal by $F/2^n \times T_{cp}$, where F is the integer value of said n-bit fractional multiple, and T_{cp} is the period of said clock signal.

29. A method according to claim 28, wherein said step of further delaying said control signal comprises the steps of:

providing said control signal to respective inputs of N delay elements, each i'th one of said delay elements inserting a respective relative delay of ((i-1)/N) T_{cp}; and

selecting an output of the F'th one of said delay elements.

30. A method according to claim 28, further comprising the step of latching said n-bit fractional multiple while said counter counts.

31. Selectable control signal delay apparatus, for use with a delay value specified as a fixed point value with m>0 integer bits carrying a value P and n>0 fraction bits carrying a value F, comprising:

a counter having a load input port, a count output port and a clock input, said load input port being coupled to receive said integer bits and said clock input being coupled to receive a clock signal having a clock period T_{cp};

a control signal generator coupled to generate said control signal in response to count completion by said counter; and

a fractional delay circuit coupled to receive said control signal and said fraction bits, said fractional delay circuit delaying said control signal by $F/2^n \times T_{cp}$.

32. Apparatus according to claim 31, wherein said fractional delay circuit comprises N delay elements each having an input coupled to receive said control signal, each i'th one of said delay elements having an output and inserting a respective relative delay of $((i-1)/N)\ T_{cp}$; and

a multiplexer coupled to receive the outputs of said N delay elements, said multiplexer further having a select input coupled to receive said fraction bits.

33. Apparatus according to claim 32, wherein the 1^{st} one of said delay elements consists of a conductor connecting the input of said 1^{st} delay element to the output of said 1^{st} delay element.

34. Apparatus according to claim 32, further comprising a storage element having an input port coupled to receive said fraction bits and an output port coupled to the select input of said multiplexer.

35. Selectable control signal delay apparatus, for use with a delay value specified as a 6-bit fixed point value, comprising:

a counter having a load input port, a count output port and a clock input, said load input port being coupled to receive the high order 5 bits of said delay value and

said clock input being coupled to receive a clock signal having a clock period;

a latch having a data input and a data output, the data input of said latch being coupled to receive the low order bit of said delay value;

a count completion detector coupled to generate a control signal in response to count completion by said counter;

a half-clock-period delay element having an input and an output, the input of said half-clock-period delay element being coupled to receive said control signal; and

a multiplexer having first and second inputs and a select input, the first input of said multiplexer being coupled to receive said control signal from said count completion detector, the second input of said multiplexer being coupled to the output of said half-clock-period delay element.